Chapter 1

Introduction of Electronic Packaging
Introduction of Electronic Packaging
Why Need Package?

IC Foundry → Packaging house → Module

Wafer → Package → Card

Back plane/Rack → Sub-system → System

Product

Empowering Innovation
Concept of Electric Packaging

- Why is Electrical Packaging Important?
- Helps Drive Moore's Law:
  Transistor Densities x2 every 18 months

Silicon Processor:
The “brain” of the computer
(generates instructions)

Packaging:
The rest of the body
(Communicates instructions to the outside world, feeds power to the processor, adds protection)

Fast silicon in a slow package is like putting a Formula One Engine in a compact car and expecting it to run like a race car.
Moore's Law:
Largely as a result of feature size shrinkage, chip power was roughly doubly every 18 months, with a concurrent reduction in cost.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Year of Introduction</th>
<th>Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>4004</td>
<td>1971</td>
<td>2,250</td>
</tr>
<tr>
<td>8008</td>
<td>1972</td>
<td>2,500</td>
</tr>
<tr>
<td>8080</td>
<td>1974</td>
<td>5,000</td>
</tr>
<tr>
<td>8086</td>
<td>1978</td>
<td>29,000</td>
</tr>
<tr>
<td>286</td>
<td>1982</td>
<td>120,000</td>
</tr>
<tr>
<td>Intel® © processor</td>
<td>1985</td>
<td>275,000</td>
</tr>
<tr>
<td>Intel® © processor</td>
<td>1989</td>
<td>1,180,000</td>
</tr>
<tr>
<td>Intel® Pentium® processor</td>
<td>1993</td>
<td>3,100,000</td>
</tr>
<tr>
<td>Intel® Pentium® II processor</td>
<td>1997</td>
<td>7,500,000</td>
</tr>
<tr>
<td>Intel® Pentium® III processor</td>
<td>1999</td>
<td>24,000,000</td>
</tr>
<tr>
<td>Intel® Pentium® 4 processor</td>
<td>2000</td>
<td>42,000,000</td>
</tr>
<tr>
<td>Intel® Itanium® processor</td>
<td>2002</td>
<td>220,000,000</td>
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<tr>
<td>Intel® Itanium® 2 processor</td>
<td>2003</td>
<td>410,000,000</td>
</tr>
</tbody>
</table>
Classification of Electronic Packaging

0-level: interconnection system
1-level (component-level): package for silicon ICs
1.5-level: direct chip on board, intermediate level between the 1- & 2-level package
2-level (board-level): package for PCB as a modulus
3-level (system-level): package for specific functional system
Purpose of IC Packaging

- IC-to PCB circuit connection and trace density relaxing
  - Example: IC pad pitch < solder bump pitch < solder ball pitch in flip-chip package

- Outline dimension standardization
  - Unity of package configuration and interconnection for convenient usage in industry (module)

- IC chip heat dissipation
  - Heat dissipation channels: conduction (> 85%), convection (10~15%) and radiation (<5%)
  - Thermal conductivity dominates PKG thermal performance

- IC chip protection
  - Mechanical strength
Birth of Electronic Packaging

- **Origin**: 1890’s census
- **Herman Hollerith**: mechanical tabulating machine derived by electrical motor that introduced the punch card (one of earliest computers)
- **ENIAC**: Electronic Numeric Integrator and Calculator, the worldwide 1st electronic computer (World War II, 1947; vacuum tube-based computer → limited operating time due to tube burnout)
- **Vacuum tube**: the first generation of electronic package (1900’s ~1950’s)

<table>
<thead>
<tr>
<th>Size, ft</th>
<th>30 x 50</th>
</tr>
</thead>
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<tr>
<td>Weight, tons</td>
<td>30</td>
</tr>
<tr>
<td>Vacuum Tubes</td>
<td>18,000</td>
</tr>
<tr>
<td>Resistors</td>
<td>70,000</td>
</tr>
<tr>
<td>Capacitors</td>
<td>10,000</td>
</tr>
<tr>
<td>Switches</td>
<td>6000</td>
</tr>
<tr>
<td>Power Requirements, W</td>
<td>150,000</td>
</tr>
<tr>
<td>Cost (in 1940)</td>
<td>$400,000</td>
</tr>
</tbody>
</table>

Vacuum Tube

two electrodes separated by a grid in a glass enclosure (vacuum); drawbacks: bulky, prone to loose connections & vacuum leaks, fragile, large power consumption, elements deteriorate rapidly

Can type package

Empowering Innovation®
IC Package History

Area Array Package Trend

- BGA (352)
- PLCC/QFP
- LQFP/QFP
- EBGAs
- LFBGA
- FC BGA (~680)
- Thermal Enhanced FC BGA
- Stack-die BGA
- MCM
- Thermal Enhanced FC BGA with Thin-Film substrate
- WL-CSP
- FC-CSP
- Image Sensor Package
- μBGA
- QFN

Pin Count / Performance

2000  2001  2002  2003

Empowering Innovation
Package Category
Category of Package Type

- **By material**
  - Ceramic
  - Epoxy mounding compound (EMC)

- **By inner interconnection (chip-to-package)**
  - Wire bonding (W/B)
  - Control collapsed chip connection (C4), flip-chip bonding (FC)
  - Tab automatic bonding (TAB)

- **By outer interconnection (package-to-PCB)**
  - Pin through hole (PTH)
  - Surface mount technology (SMT)

- **By chip carrier material**
  - Leadframe
  - Substrate
General Classification

... by configuration

- Standard Type
  - DIP (Dual in-line Package)
  - ZIP (Zigzag in-line Package)
  - SIP (Single in-line Package)
  - PGA (Pin Grid Array)
  - S-DIP (Shrink DIP)
- Shrink Type
  - SOP (Small Outline Package)
  - TSOP (Thin Small Outline Package)
  - HSOP (SOP with Heat Sink)
  - QFP (Quad Flat Package)
  - TQFP (Thin Quad Flat Package)
  - HQFP (QFP with Heat Sink)
  - BQFP (QFP with Bumper)
  - GQFP (QFP with Guard Ring)
- Wing Type
  - QFP (Small Outline J-ledged Package)
  - HQFP (SOJ with Heat Sink)
  - SOJ (Quad Flat J-ledged Package)
  - HQFI (Small Outline I-ledged Package)
  - SOI (SOI with Heat Sink)
  - HSOI (Quad Flat I-ledged Package)
- Leadless Type
  - QFN (Quad Flat Non-ledged Package)
  - BGA (Ball Grid Array)
  - TCP (TAB) (Tape Carrier Package)
  - EBN (Tape Automatic Bonding)

American Electronic Components Joint Council, JEDEC
Electronic Industry Association of Japan, EIAJ
International Electrotechnical Commission, IEC
Dual Family:
Consumer Application, Game, Power Device, Memory

PDIP/SPDIP
Plastic/Shrink Dual In-Line Package

SOIC / SOJ
Small Outline IC Package

SSOP
Shrink Small Outline Package

TSOP
Thin Small Outline Package
Quad Family:
RF, CDROM, Communication

**PLCC**
Plastic Leaded Chip Carrier Package

**QFN**
Quad Flat Non-Lead Package

**TQFP**
Thin Quad Flat Pack Package

**QFP**
Quad Flat Pack Package

**LQFP**
Low Profile Quad Flat Pack
Chip Scale Package Family:
Memory, Cellular Chipset

CSP
Chip Scale Package

BGA-T
Tape BGA Package

uBGAR
microBGA Package

fcCSP
FlipChip Chip Scale Package
BGA Family:
Chipset, Graphics, Network Processor

PBGA
Plastic Ball Grid Array Package

LFBGA
Low Profile Ball Grid Array

Flip Chip
Flip-Chip Package

SBGA/VBGA
Super/Viper BGA Package

Empowering Innovation
Real estate efficiencies of packages of various types for surface mounting. (Intel Corporation.)
Electronic Product Categories

- **Low-Cost** <$300:
  - disk drives, micro-controllers, VCR’s
- **Hand-Held** < $700: PDA’s, cellular phones
- **Cost/Performance** <$2000:
  - PC’s, Notebooks, Telecom
- **High-Performance** > $3000:
  - Servers, Supercomputers, Routers, Switches
- **Harsh Environment:**
  - Automotive, Military, Avionics, Space
Package Structure Design
How to determine a Package structure?

- **PKG pin count number**
  - (Rent’s rule)
  
  \[ I/O \text{ number} = (n - 1)\sqrt{N} \]
  
  \( n \): divergence of CMOS transistor  \( N \): total transistor number

- **Applications**
  - PKG families (dual, quad, chip scale, BGA, TAB)

- **Packaging dimensions**
  - Physical / geometrical constraints

- **Thermal performance**
  - Thermal resistance (Theta-jc, Theta-jb & Theta-ja)

- **Mechanical performance**
  - Warpage, solder fatigue life

- **Electrical performance**
  - Signal and power integrity

- **Cost**
The Circuit Configuration of a CMOS Output Buffer

Complementary Metal Oxide Semiconductor

- Drain-source resistance
- First incident voltage

\[ R_s = \frac{V_{OL}}{I_d} \]

\[ V_{fi} = \frac{Z_0}{Z_0 + R_s} V_{CC} \]
Three Legs of Package

- Weibull distribution
- Design for reliability (DFR)
- Optimization
  Reliable package
- Reliability testing and data analysis (RTDA)
- Material & structure
  Computer aid engineering (CAE)
- ANSYS, ABQUS, LsDYNA
- IcePAK, Fluent
- Failure mode effective analysis (FMEA)
- Optimization
  Reliable package
- Design for reliability (DFR)
- Reliability testing and data analysis (RTDA)
- Material & structure
  Computer aid engineering (CAE)
- ANSYS, ABQUS, LsDYNA
- IcePAK, Fluent
- Failure mode effective analysis (FMEA)
Design for Reliability

1. Design
2. Build Models
3. Analyze Stress
4. Predict Life
5. Optimize Design
6. Characterize Factors
7. Validate Models

- Delamination/Crack Modeling Potential
- Integration with Thermal & Electrical Modeling
## Typical Package Reliability items

<table>
<thead>
<tr>
<th>Test Items</th>
<th>Sample Size</th>
<th># of Lots</th>
<th>Read out (hrs/cys)</th>
<th>Lot Acc/SS</th>
<th>Cum. Acc/SS</th>
<th>Test Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Cycling</td>
<td>77/lot (LTPD 5%)</td>
<td>3</td>
<td>200/500 (spec) and 1000 cys (ref.)</td>
<td>1/77 (LTPD 5%)</td>
<td>2/231</td>
<td>MIL-STD-883E, M1010, Cond.B, Cond.C (ref.)</td>
</tr>
<tr>
<td>- -55°C to 125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- -65°C to 150°C (ref.) (Air to Air)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Humidity Test</td>
<td>77/lot (LTPD 5%)</td>
<td>3</td>
<td>500/1000 hours</td>
<td>1/77 (LTPD 5%)</td>
<td>2/231</td>
<td>JEDEC-STD-22-A101-A w/o bias</td>
</tr>
<tr>
<td>- 85°C/85%RH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pressure Cooker Test</td>
<td>77/lot (LTPD 5%)</td>
<td>3</td>
<td>96/168 hours</td>
<td>1/77 (LTPD 5%)</td>
<td>2/231</td>
<td>JEDEC-STD-22-A102-B</td>
</tr>
<tr>
<td>- 121°C/100%RH/2 ATM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High Temperature Storage Test</td>
<td>77/lot (LTPD 5%)</td>
<td>3</td>
<td>500/1000 hours</td>
<td>1/77 (LTPD 5%)</td>
<td>2/231</td>
<td>MIL-STD-883E, M1008</td>
</tr>
<tr>
<td>- 150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pre-conditioning (level 3) Test</td>
<td>32/lot</td>
<td>3</td>
<td>Note (1) (LTPD 7%)</td>
<td>0/32</td>
<td>0/96</td>
<td>JEDEC-STD-22-A113-A</td>
</tr>
</tbody>
</table>

Note (1): Pre-conditioning flow: C-SAM --> T/C 5 cycle (cond.C) --> Bake (125°C, 24 hrs) --> TH Soak 30°C/60%RH, 192 hrs --> IR*3 --> C-SAM. The failure criteria is larger than 5% delamination on die area.

22/lot: evaluation qualification (engineering)
77/lot: formal qualification (release to production)
Typical Assembly Process Qualification Items

- Die Shear Strength Test
  (MIL-STD-883, M2019)
- Epoxy Thickness Measurement
- Wire Pull Strength Measurement
  (MIL-STD-883, M2011)
- Ball Shear Test
  (JEDEC Standard 22-B116)
- Bond Pad Cratering Test
- Post Mold X-Ray Inspection
Typical Assembly Process Qualification Items

- Solderability Test
  (MIL-STD-883, M2019)
- Solder Plating Thickness Test
  (MIL-STD-38510)
- Sn/Pb Composition Test
  (MIL-STD-38510)
- Mark Permanance Test
  (MIL-STD-883, M2019)
- Lead Coplanarity
  (JEDEC STD, No.95)
- Lead Fatigue Test
Process Interaction on Failure Mechanisms

![Diagram showing the interaction of different processes affecting failure mechanisms.]

- Wafer Process
- Die Design
- Assembly Process
- Customer Board Design
- Board Mounting Process

Failure Mechanism

Failure Mode

Environmental Stress Testing
Failure Analysis Procedure

**FAILURE ANALYSIS PROCEDURE**

1. **OCCURRENCE OF FAILURE**
2. **VERIFICATION THRU DOCUMENTS RECORDS**
3. **EXTERNAL VISUAL CHECK**
4. **ELECTRICAL TEST**
5. **SOFTX-RAY EXAMINATION**
6. **V-1 CHARACTERISTIC EXAMINATION**

**OPTION:**

- **DIE PENETRATION TEST**
- **SAT**
- **DECAP**
- **CROSS-SECTION**

**INTERNAL MICRSCOPIC OBSERVATION**
- **OPTICAL**
- **SEM**

**EXAMINATION ANALYSIS OF CAUSE & FAILURE MECHANISM**

**DISCUSSION OF ANALYZED RESULTS**

Empowering Innovation
Bathtub Curve

- Early Failure Rate (EFR)
- Stable Failure Rate (SFR)
- Wear-out Failure Rate (WFR)

Unit: ppm/Khrs
Market Tendency
Sale Revenues of IC Industry

IC PACKAGING REVENUES 2007

IC Revenues - $205Bn

Silicon Value $177.9Bn (86.8%)

Through Hole Packages (DIP, SOT, SIP/ZIP) $0.26Bn (1%)

Merchant 24% Captive 76%

Array Packages (BGA, CSP, PGA) $16.34Bn (60%)

Merchant 31% Captive 69%

Surface Mount Packages (SO, PLCC, QFP, TAB, other) $10.5Bn (39%)

BGA $6.84Bn (42%)

Merchant 48% Captive 52%

PGA $1.6Bn (10%)

Merchant 10% Captive 90%

FC/Wafer CSP $2.6Bn (16%)

Merchant 15% Captive 85%

CSP $5.3Bn (32%)

Merchant 60% Captive 40%
# Roadmap of Assembly Market

## Market Roadmap

### 2003
- Memory: 14M 8%
- DSP: 13M 7%
- Graphics: 17M 9.4%
- Chipset/MPR: 95M 54%
- ASIC/Logic: 25M 14%

Total: 186M Units

### 2007
- Memory: 38M 4%
- MPU/MCU: 50M 7%
- DSP: 76M 11%
- Graphics: 137M 20%
- Chipset/MPR: 288M 42%
- ASIC/Logic: 101M 15%

Total: 682M Units

## Actuals and Forecasts of Subcontract Assemblers and Foundries

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Top Assemblers</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Amkor</td>
<td>350</td>
<td>400</td>
<td>450</td>
<td>472</td>
<td>14%</td>
<td>3%</td>
</tr>
<tr>
<td>ASE</td>
<td>330</td>
<td>416</td>
<td>544</td>
<td>566</td>
<td>26%</td>
<td>4%</td>
</tr>
<tr>
<td>SYP</td>
<td>160</td>
<td>201</td>
<td>242</td>
<td>240</td>
<td>26%</td>
<td>-1%</td>
</tr>
<tr>
<td>ChipPAC</td>
<td>91</td>
<td>107</td>
<td>128</td>
<td>128</td>
<td>18%</td>
<td>0%</td>
</tr>
<tr>
<td>OSE</td>
<td>92</td>
<td>98</td>
<td>120</td>
<td>100</td>
<td>7%</td>
<td>-17%</td>
</tr>
<tr>
<td>STATS</td>
<td>56</td>
<td>95</td>
<td>120</td>
<td>126</td>
<td>70%</td>
<td>5%</td>
</tr>
<tr>
<td>Carsem</td>
<td>57</td>
<td>60</td>
<td>65</td>
<td>65</td>
<td>5%</td>
<td>0%</td>
</tr>
<tr>
<td>ASAT</td>
<td>37</td>
<td>42</td>
<td>48</td>
<td>53</td>
<td>14%</td>
<td>10%</td>
</tr>
<tr>
<td>AIT</td>
<td>28</td>
<td>26</td>
<td>27</td>
<td>26</td>
<td>-7%</td>
<td>-4%</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>1,201</strong></td>
<td><strong>1,445</strong></td>
<td><strong>1,753</strong></td>
<td><strong>1,776</strong></td>
<td>20%</td>
<td>1%</td>
</tr>
</tbody>
</table>

## Foundries

<table>
<thead>
<tr>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC</td>
<td>1,200</td>
<td>1,468</td>
<td>1,704</td>
<td>1,738</td>
<td>22%</td>
<td>2%</td>
</tr>
<tr>
<td>UMC</td>
<td>490</td>
<td>617</td>
<td>700</td>
<td>710</td>
<td>26%</td>
<td>1%</td>
</tr>
<tr>
<td>Chartered</td>
<td>112</td>
<td>138</td>
<td>183</td>
<td>224</td>
<td>23%</td>
<td>22%</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>1,802</strong></td>
<td><strong>2,223</strong></td>
<td><strong>2,587</strong></td>
<td><strong>2,672</strong></td>
<td><strong>23%</strong></td>
<td><strong>3%</strong></td>
</tr>
</tbody>
</table>

**Note:** All values are converted to USS based on average exchange rates for any given quarter.
### Worldwide IC Packaging Market Forecast

<table>
<thead>
<tr>
<th>IC Packages</th>
<th>1998</th>
<th>1999</th>
<th>2000</th>
<th>2001</th>
<th>2002</th>
<th>2003</th>
<th>CAGR</th>
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<tbody>
<tr>
<td>DIP</td>
<td>9548</td>
<td>8750</td>
<td>7758</td>
<td>7322</td>
<td>6707</td>
<td>6564</td>
<td>-7.22%</td>
</tr>
<tr>
<td>SO</td>
<td>34264</td>
<td>37160</td>
<td>39898</td>
<td>43138</td>
<td>46796</td>
<td>50454</td>
<td>8.05%</td>
</tr>
<tr>
<td>CC</td>
<td>3568</td>
<td>3694</td>
<td>3822</td>
<td>4001</td>
<td>4266</td>
<td>4594</td>
<td>5.18%</td>
</tr>
<tr>
<td>QFP</td>
<td>5702</td>
<td>6427</td>
<td>7336</td>
<td>8277</td>
<td>9367</td>
<td>10391</td>
<td>12.75%</td>
</tr>
<tr>
<td>PGA</td>
<td>219</td>
<td>251</td>
<td>295</td>
<td>338</td>
<td>414</td>
<td>497</td>
<td>17.83%</td>
</tr>
<tr>
<td>BGA</td>
<td>1828</td>
<td>3078</td>
<td>5083</td>
<td>7010</td>
<td>9228</td>
<td>12290</td>
<td>46.39%</td>
</tr>
<tr>
<td>DCA</td>
<td>3588</td>
<td>4001</td>
<td>4459</td>
<td>5010</td>
<td>5721</td>
<td>6508</td>
<td>12.65%</td>
</tr>
<tr>
<td>Total</td>
<td>58716</td>
<td>63361</td>
<td>68656</td>
<td>75096</td>
<td>82499</td>
<td>91299</td>
<td>9.23%</td>
</tr>
</tbody>
</table>

*This table shows the IC packaging market. "IC packaging" is a total of the IC packaging industry. Source: The Worldwide IC Packaging Market, 1999 Edition Electronic Trend Publications, Inc.*

### IC Packaging Revenue Forecast

<table>
<thead>
<tr>
<th></th>
<th>1998</th>
<th>1999</th>
<th>2000</th>
<th>2001</th>
<th>2002</th>
<th>2003</th>
<th>CAGR</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP</td>
<td>1081</td>
<td>922</td>
<td>744</td>
<td>653</td>
<td>566</td>
<td>546</td>
<td>-12.76%</td>
</tr>
<tr>
<td>SO</td>
<td>4689</td>
<td>4879</td>
<td>4891</td>
<td>5076</td>
<td>5148</td>
<td>5298</td>
<td>2.47%</td>
</tr>
<tr>
<td>CC</td>
<td>1161</td>
<td>1186</td>
<td>1209</td>
<td>1221</td>
<td>1297</td>
<td>1306</td>
<td>2.37%</td>
</tr>
<tr>
<td>QFP</td>
<td>3739</td>
<td>4029</td>
<td>4351</td>
<td>4612</td>
<td>5067</td>
<td>5384</td>
<td>7.56%</td>
</tr>
<tr>
<td>PGA</td>
<td>1858</td>
<td>2271</td>
<td>2677</td>
<td>3060</td>
<td>3776</td>
<td>4505</td>
<td>19.38%</td>
</tr>
<tr>
<td>BGA</td>
<td>3628</td>
<td>4916</td>
<td>6560</td>
<td>8288</td>
<td>9957</td>
<td>12075</td>
<td>27.10%</td>
</tr>
<tr>
<td>DCA</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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</tr>
<tr>
<td>Total</td>
<td>16158</td>
<td>18198</td>
<td>20423</td>
<td>22910</td>
<td>25810</td>
<td>29114</td>
<td>12.50%</td>
</tr>
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</table>

*This table shows the IC packaging market. "IC packaging revenue" is the total value of the IC packaging industry. Source: The Worldwide IC Packaging Market, 1999 Edition Electronic Trend Publications, Inc.*
### Worldwide Contract Packaging Market Forecast

<table>
<thead>
<tr>
<th>Contract Packaging Units</th>
<th>1998</th>
<th>1999</th>
<th>2000</th>
<th>2001</th>
<th>2002</th>
<th>2003</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP</td>
<td>2009</td>
<td>2190</td>
<td>2343</td>
<td>2460</td>
<td>2583</td>
<td>2660</td>
</tr>
<tr>
<td>SO</td>
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<td>5881</td>
<td>6469</td>
<td>7051</td>
<td>7686</td>
<td>8378</td>
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<tr>
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<td>1054</td>
<td>1065</td>
<td>1075</td>
<td>1086</td>
<td>1097</td>
</tr>
<tr>
<td>QFP</td>
<td>2265</td>
<td>2491</td>
<td>2740</td>
<td>3014</td>
<td>3316</td>
<td>3647</td>
</tr>
<tr>
<td>PGA</td>
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<td>32</td>
<td>29</td>
<td>27</td>
<td>26</td>
<td>24</td>
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<td>2544</td>
<td>3561</td>
<td>4629</td>
<td>6018</td>
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<tr>
<td><strong>Total</strong></td>
<td><strong>11533</strong></td>
<td><strong>13237</strong></td>
<td><strong>15189</strong></td>
<td><strong>17189</strong></td>
<td><strong>19325</strong></td>
<td><strong>21824</strong></td>
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</tbody>
</table>


### Contract Packaging Revenue Forecast

<table>
<thead>
<tr>
<th>Contract Packaging Units</th>
<th>1998</th>
<th>1999</th>
<th>2000</th>
<th>2001</th>
<th>2002</th>
<th>2003</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP</td>
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<td>294</td>
<td>276</td>
<td>256</td>
<td>245</td>
<td>235</td>
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<tr>
<td>SO</td>
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<tr>
<td>CC</td>
<td>363</td>
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<tr>
<td>QFP</td>
<td>1997</td>
<td>2070</td>
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<td>2170</td>
<td>2269</td>
<td>2327</td>
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<tr>
<td>PGA</td>
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<td>314</td>
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<td>216</td>
<td>196</td>
<td>180</td>
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<tr>
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<td>3161</td>
<td>4350</td>
<td>5600</td>
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<td>8573</td>
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<tr>
<td><strong>Total</strong></td>
<td><strong>6143</strong></td>
<td><strong>7251</strong></td>
<td><strong>8494</strong></td>
<td><strong>9757</strong></td>
<td><strong>11228</strong></td>
<td><strong>12942</strong></td>
</tr>
</tbody>
</table>

Strategical alliance with front-end foundry houses
- Ally with foundry houses to be a co-developing relationship
- Secure the production capacity from allied foundry houses
- Maintain the leading position of the cutting edge technology

Mergence fashion
- Massive economic of scale
- Discontinuity of packaging technology
- Low cost, high quality and worldwide business capability

Advanced packaging technology
- Advanced technology equal to high profit
- Align with the development of IC technology (Moore’s law)
- Increase the gap distance between the competitors
- Flip-chip technology becomes the mainstream technology
Growth and Stimulation of Backend Business

分析封測成長動力流程示意圖

2003年
1. 臺灣封測產值1585E (Y0Y 24.1%) = 封裝1176E + 測試409E
2. 臺灣封測產業全球市佔率約四成

観察重點：
臺灣IC design庫存問題

2004年
1. 臺灣封測產值2064E (Y0Y 30%) = 封裝1511E + 測試553E
2. 臺灣封測產業市佔率小幅成長

E：億新台幣
Source：拓墣產業研究所，2004/09